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The Vital role of CMOS Logic Gate in CMOS Technology

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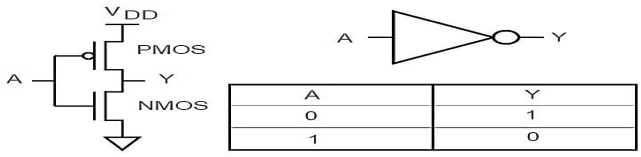
ABSTRACT
Process parameters have changed drastically as a result of CMOS technology's quick scalability. Since various transistor configurations exhibit distinct electrical properties, this study examines how process variability affects logic gate performance based on topology and the switching device's relative location within the network.

KEYWORDS
CMOS, MOSFETs, Gate, Logic, Transistor.

INTRODUCTION
The fundamental components of Logic gates are used in all digital circuits and computers. Transistors known as MOSFETs are used to implement these logic gates. One type of voltage-controlled switch is a MOSFET transistor. When the voltage on the MOSFET is high or low, it functions as a switch and turns on or off. MOSFETs come in two varieties: NMOS and PMOS. When the voltage is elevated, the NMOS activates, and when the voltage is lower, it deactivates. In contrast, the PMOS activates when there is a low voltage and deactivates when there is a high voltage. They are referred to as CMOS (Complementary MOS) when they are utilized in tandem to create logic gates. NMOS and PMOS function in a complementary manner, which is why they are referred to as complementary. The PMOS switches off when the NMOS switch is turned on, and the other way around.

CMOS Inverter
Below is a picture of the CMOS inverter. It is made up of an NMOS and a PMOS connected in series. Ground is the symbol for logic 0, whereas VDD is the symbol for logic one. The NMOS are activated and the PMOS are turned off when the input increase or 1. Consequently, output Y becomes logic 0 since it is directly connected to ground. When the input is logic 0, the opposite occurs: PMOS turns on and NMOS turns off. Consequently, output Y and VDD have a direct path. Therefore, Y rises. This is the fundamental way that a CMOS inverter works.



A	Y
0	1
1	0

Figure (1) - Structure of CMOS Inverter
(GeeksforGeeks(2024);https://www.geeksforgeeks.org/digital-logic/cmos-logic-gate/

According to the aforementioned analysis, a circuit for switching including switches for PMOS in the top block that turn on when the inputs are decrease and the bottom block's NMOS switches that activate when the inputs are high is required to implement any boolean function using CMOS technology. There must be a complementary relationship between the two blocks. Pull-up networks (PUNs) are made up of solely PMOS in the top block, which raises the output to logic high or VDD. Due to the fact that it draws the output to ground or logic low, the bottom block made up of NMOS is known as a pull-down network (PDN). PUN and PDN can be used to realize any Boolean function.

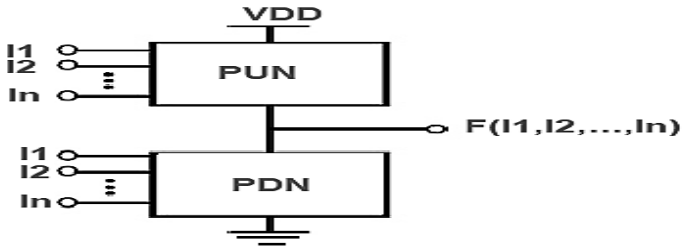


Figure (2) - Structure of PUN and PDN (GeeksforGeeks (2024); https://www.geeksforgeeks.org/digital-logic/cmos-logic-gate/).

Let's say that Y = F (A, B, C, D). The PDN and PUN blocks must be extracted from the provided Boolean expression. We must acquire the non-complementary variables A, B, C, and D with relation to Y' in order to obtain the PDN block. Two NMOS in series to ground are indicated if AND is present in the expression of Y'. Two NMOS are operating in parallel if there is an OR. In terms of the supplemented variables A', B', C', and D', we require Y for the PUN. Again, two PMOS in series are required if AND is included in the expression of Y, and two PMOS in parallel are indicated by an OR.

AOI Gate and OAI Gate

CMOS logic can be used to implement two fundamental configurations: AOI (and-or-invert) and OAI (or-and-invert) gates. These two kinds of gates' CMOS implementations are displayed below. The two gates are dual to one another, as you can see. The structural similarities between the PDN of the AOI gate and the PUN of the OAI gate are evident, as is the structural similarity between the two gates.

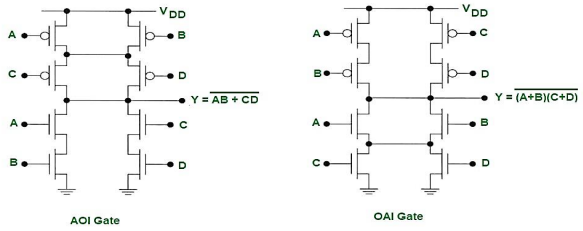


Figure (3) - Structure of AOI Gate and OAI Gate (GeeksforGeeks (2024); https://www.geeksforgeeks.org/digital-logic/cmos-logic-gate/).

Complementary Metal Oxide Semiconductor (CMOS)

The intial benefit of CMOS technology over NMOS and BIPOLAR is the noticeably reduced dissipation of power. Complementary MOS circuits differ from NMOS or BIPOLAR circuits, circuits dissipate nearly zero-static power. Only when the circuit truly switches does power drain. This makes it possible to integrate more CMOS gates on an IC, which improves performance significantly when compared to NMOS or bipolar technology. There are two varieties of semiconductor transistors with complementary metal oxides: N-channel MOS and P-channel MOS.

The CMOS Operating Principle

Regarding CMOS technology, logic functions are built and utilizing both N-type and P-type transistors. The identical signal which converts on 1-kind of transistor can also be utilized to turn it off. This feature makes it possible to make logic devices without a voltage divider, and fundamental switches. A group of n-kind MOSFETs is positioned in a pulled down network between the output and the power supply line with low voltage (Vss or, more frequently, ground) in CMOS logic gates. CMOS logic gates employ a team of p-kind MOSFETs within a pull-up network that connects the output and the higher-voltage rail (generally known as Vdd) rather than the existing dynamic braking resistor in NMOS logic gates.

CMOS's fabrication

these silicon wafer can be used to fabricate CMOS transistors. The wafer's diameter is between 20 and 300 mm. The printing press and the lithography process are identical in this regard. At each step, various contents can be etched, incorporated, or alternatively. These procedures can be easily understood by seeing the wafer's top and alternative section utilizing a condensed assembly approach. Three technologies can be utilized to create CMOS: N-well pt P-well, Twin well, and an SOI (Silicon on Insulator).

Advantages

1. Good noise margin and lower power consumption are CMOS's primary advantages over TTL. This is because there isn't a straight path of conductivity between VDD and GND. The digital signal can then be transmitted easily and affordably using CMOS devices, with fall times depending on input conditions.
2. The quantity of motherboard memory that will be kept in the BIOS settings is described by CMOS. These settings mostly consist of the hardware settings, date, and time. Bipolar transistors in a TTL digital logic circuit operate on DC pulses. Typically, a single integrated circuit (IC) contains many transistor logic gates.

Applications for CMOS

For almost all digital logic applications, complementary MOS processes have essentially supplanted NMOS and bipolar processes due to their widespread implementation. These designs for digital ICs has been made using CMOS-

i. Central processing unit and Computer main memory
ii. Microprocessors Designs
iii. Semi-Conductor Memory Design
iv. Application-specific integrated circuits (ASICs) are designed using this method.

CONCLUSION

Because of their scalability, high noise immunity, and low power consumption, CMOS logic gates are essential in contemporary electronics. CMOS is perfect for processors and memory devices because it minimizes static power dissipation by using both NMOS and PMOS transistors. Even if design and fabrication present difficulties, performance is continuously improved by developments like FET and 3D chip stacking. All things considered, CMOS technology will continue to play a key role in upcoming advancements in computing and digital systems.

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